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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,858	03/03/2004	Toshitaka Tatsunari	60188-791	3092

7590 03/03/2005  
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EXAMINER
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LE, THAO P

ART UNIT	PAPER NUMBER
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2818

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/790,858	<b>Applicant(s)</b> TATSUNARI, TOSHITAKA	
	<b>Examiner</b> Thao P. Le	<b>Art Unit</b> 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 19 January 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>1 page</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. This office action is responsive to communication(s) filed on 01/19/2005.  
Claims 1-18 are presented for examination including new additional claims.  
Claims 1-11 and 13-14 have been amended.

### ***Information Disclosure Statement***

2. The information disclosure statement (IDS) submitted on 1/19/2005 was filed after the mailing date of the application. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.
3. Applicant's arguments with respect to amended independent claims 1 and 7 have been considered but are moot in view of the new ground(s) of rejection.

Applicants argue that Takumi doesn't suggest or teach the limitations of claims 1 and 7, as amended, recited a semiconductor device and method of making the device wherein a lower surface of the capacitive insulating film is in contact with the first insulating film. Examiner agreed with applicant's traversal, however, in view of the new cited art, Nagano et al (U.S. Patent No. 6,730,951) discloses a semiconductor device

wherein a lower surface of the capacitive insulating film 32 is in contact with the first insulating film 16 (See Figs. 1-14).

4. Claims 1-18 are rejected under 35 U.S.C. 103(a) as following:

**Claim Rejections - 35 USC § 103**

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1, 3-4, 7, 8-10, 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takumi, Japan Application No. 2001257532 (submitted by applicant as prior art), in view of Nagano et al., U.S. Patent No. 6,730,951.

Regarding claims 1 and 7, Takumi discloses a semiconductor device and method of making the semiconductor device comprising:

a first hydrogen barrier film 8 formed over a substrate;

a capacitive lower electrode 7 formed on the first hydrogen barrier film;

a first insulating film 15 formed on the first hydrogen barrier film to cover a side of the capacitive lower electrode;

a capacitive insulating film 9 comprising an insulating metal oxide and formed on the capacitive lower electrode;

a capacitive upper electrode 10 formed on the insulating film;

a second insulating film 15E formed on the first insulating film to cover the capacitive insulating film and the capacitive upper; and

a second hydrogen barrier film 11 formed on the second insulating film.

Takumi fails to disclose wherein a lower surface of the capacitive insulating film 9 is in contact with the first insulating film 15. However, Nagano et al. discloses a semiconductor device similar to Takumi's and further discloses wherein the lower surface of the capacitive insulating film 32 is in contact with the first insulating film 16 (Fig. 3B). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the capacitive insulating film on and in contact with the first insulating film as taught in Nagano et al. because the diameter of the lower electrode in the direction of the substrate plane is smaller than that of the capacitive insulating film, the first insulating film is formed on the sides of the lower electrode and in contact with the capacitive film in order to fill in the gap between the capacitive insulating film and hydrogen barrier layer for insulation and to surround the lower electrode for electrically insulating adjacent ones of the lower electrodes.

Regarding claim 3, Takumi and Nagano et al. disclose the limitations of claim 1 and further disclose wherein the capacitive insulating film comprises a ferroelectric film, and the capacitor structure is covered with the first and second hydrogen barrier films (Fig. 3B of Nagano et al.).

Regarding claim 4, Takumi and Nagano et al. disclose the limitations of claim 1 and Nagano et al. further discloses wherein a side of the first hydrogen barrier film is connected to the second hydrogen barrier film so that the capacitive lower electrode, the capacitive insulating film and the capacitive upper electrode are covered with the first and second hydrogen barrier films (Fig. 3B of Nagano et al.)

Regarding claims 8-9, Takumi and Nagano et al. disclose the limitations of claim 7, and Takumi further discloses the step of forming a sloped portion in the second insulating film at a position corresponding to an edge of the upper electrode, between the step of forming the second insulating film and the step of forming the second hydrogen barrier layer wherein the sloped portion is formed by sputtering on the second film with inert ions or etching the entire surface of the second insulating film (Figs. 15-16).

Regarding claim 10, Takumi and Nagano et al. disclose the limitations of claim 1 and Takumi discloses the step of forming a loped portion in the second insulating film at a position corresponding to an edge of the upper electrode, between the step of forming the second insulating layer and second hydrogen barrier layer by etching the second insulating film and first insulating film into an island shape and Nagano et al. further discloses wherein a side of the first hydrogen barrier film is connected to the second

hydrogen barrier film so that the capacitive lower electrode, the capacitive insulating film and the capacitive upper electrode are covered with the first and second hydrogen barrier films (Fig. 3B of Nagano et al.)

Regarding claim 15, Takumi and Nagano et al. disclose the limitations of claim 1 and Nagano et al. further discloses wherein the size of the capacitive insulating film is larger than that of the capacitive lower electrode (See Fig. 3B).

Regarding claim 16, Takumi and Nagano et al. disclose the limitations of claim 1 and Nagano et al. further discloses wherein the upper surface of the lower electrode is flush with the upper surface of the first insulating film (Fig. 3B).

Regarding claims 17-18, Takumi and Nagano et al. disclose the limitations of claim 1 and Nagano et al. further discloses wherein a conductive film comprises TiN formed between the first hydrogen barrier layer and the lower electrode (Fig. 9B-9C; lines 59-67, Col. 27).

7. Claim 5, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takumi, Japan Application No. 2001257532, in view of Nagano et al., U.S. Patent No. 6,730,951, and further in view of AAPA (Applicant Admitted Prior Art).

Regarding claims 5 and 14, Takumi and Nagano et al. disclose the limitations of claims 1 and 7 but fail to disclose wherein the lower electrode comprises a multilayer film in which a TiAlN film, an Ir film, and IrO<sub>2</sub> film, and a Pt film are stacked in this order. However, AAPA discloses a semiconductor device wherein the lower electrode

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comprises a multilayer film in which a TiAlN film, an Ir film, and IrO<sub>2</sub> film, and a Pt film are stacked in this order (page 2, Fig. 11). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the lower electrode comprising multi film of a TiAlN film, an Ir film, and IrO<sub>2</sub> film, and a Pt film in order to prevent oxygen from being diffused into the underlying contact plug and prevent the diffusion of hydrogen from the lower electrode into the capacitive insulating layer.

8. Claims 2, 6, 11, 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takumi, Japan Application No. 2001257532 (submitted by applicant as prior art), in view of Nagano et al., U.S. Patent No. 6,730,951, and further in view of Hikosaka et al., U.S. Patent No. 6,706,540.

Regarding claims 2 and 11, Takumi discloses a semiconductor device and method of making the semiconductor device comprising:

Regarding claims 2 and 11, Takumi discloses a semiconductor device and method of making the semiconductor device comprising:

- a first hydrogen barrier film 8 formed over a substrate;
- a capacitive lower electrode 7 formed on the first hydrogen barrier film;
- a first insulating film 15 formed on the first hydrogen barrier film to cover a side of the capacitive lower electrode;
- a capacitive insulating film 9 comprising an insulting metal oxide and formed on the capacitive lower electrode;
- a capacitive upper electrode 10 formed on the insulating film;



a second insulating film 15E formed on the first insulating film to cover the capacitive insulating film and the capacitive upper; and  
a second hydrogen barrier film 11 formed on the second insulating film.

Takumi fails to disclose wherein a lower surface of the capacitive insulating film 9 is in contact with the first insulating film 15. However, Nagano et al. discloses a semiconductor device similar to Takumi's and further discloses wherein the lower surface of the capacitive insulating film 32 is in contact with the first insulating film 16 (Fig. 3B). It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the capacitive insulating film on and in contact with the first insulating film as taught in Nagano et al. because the diameter of the lower electrode in the direction of the substrate plane is smaller than that of the capacitive insulating film, the first insulating film is formed on the sides of the lower electrode and in contact with the capacitive film in order to fill in the gap between the capacitive insulating film and hydrogen barrier layer for insulation and to surround the lower electrode for electrically insulating adjacent ones of the lower electrodes.

Still regarding claims 2 and 11, both Takumi and Nagano et al. fail to disclose a third insulating film formed to cover the second insulating film.

Hikosaka et al. discloses a semiconductor device and method of forming the semiconductor device with a hydrogen barrier layer comprising the use of double insulating films, the third insulating film formed to cover the second insulating film (layers 19, 21, 23, 24, Figs. 1H-1K). Hikosaka et al. also discloses the formation of

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hydrogen barrier layer 30b over the insulating layers 19, 21, 23, and 24. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Takumi and Nagano et al. in view of Hikosaka et al. to form more than one insulating films on the upper electrode before forming hydrogen barrier because more than one insulating films would prevent better of ions diffusing and better insulation, the larger process degradation suppressing effect of the capacitor can be achieved, thus the better improvement of the device characteristics.

Regarding claims 6, 12, Hikosaka et al. discloses the third insulating film comprises an undoped silicon oxide film (layers 21, 24, Fig. 1K; line 59-60, Col. 8).

Regarding claim 13, Takumi discloses the step of reflowing the second insulating film so that a portion of the second insulating corresponding to an edge of the upper electrode is rounded but fails to disclose the reflowing the third insulating film since Takumi device doesn't include the third insulating film. Hikosaka et al. discloses the device includes the third insulating film. It would have been obvious to one having ordinary skill in the art at the time the invention was made to perform a reflowing process on the third insulating film as Takumi taught the reflowing process of the second insulating film if Takumi's device had comprised the third insulating film because reflowing process is performed on a single insulating film or multi layer insulating film before forming the second hydrogen barrier layer would improve the coverage of the second hydrogen layer 11 at the edge of the capacitor structure (see Figs. 15-16 of Takumi). Still regarding to claim 13, Nagano et al. further discloses wherein a side of

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the first hydrogen barrier film is connected to the second hydrogen barrier film so that the capacitive lower electrode, the capacitive insulating film and the capacitive upper electrode are covered with the first and second hydrogen barrier films (Fig. 3B of Nagano et al.)

9. When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

### ***Conclusion***

10. For the above reasons, it is believed that the rejections should be sustained. Feature of an invention not found in the claims can be given no patentable weight in distinguishing the claimed invention over the prior art.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP ' 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

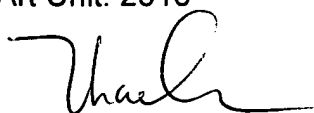
Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1787. Other inquiries of this application should be called to (571) 272-1562 or the fax number (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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A handwritten signature in black ink, appearing to read 'Thao P. Le', with a stylized, flowing script.

Thao P. Le  
Examiner  
AU 2818